CMOS-based Active Gate Drive Circuit with User-Defined Miller Drive Strength Profiles and High Resolution DPWM Circuit Design

Two critical circuits required of active gate drivers (AGD) for power discretes (MOSFET, GaN, SiC, etc.) are introduced. Several novel circuit design techniques in the said two critical circuits, namely AGD with Miller plateau detection and DPWM (digital PWM), have been proposed and then proved on silicon to justify the expected performance. Power-effective design guidelines for future AGDs will then be disclosed.